IN THE CLAIMS

Please amend claims 1, 8 and 15 as set forth below.

The text of all pending claims, along with their current status, is set forth below:

1. (Currently amended) A notification mechanism, comprising:

a plurality of completion queue handlers associated with a communication device, each of the plurality of completion queue handlers associated with a process; and

at least one completion queue associated with each one of the plurality of completion queue handlers, wherein the plurality of completion queue handlers are segregated to target processors, and wherein the segregation of the plurality of completion queue handlers is adapted to reduce cache line invalidation, cache line eviction, and/or unnecessary memory bus overhead associated with synchronization of accesses to the memory.

2. (original) The notification mechanism set forth in claim 1, wherein the process is associated with at least one processor.

3. (original) The notification mechanism set forth in claim 2, wherein each of the plurality of completion queue handlers generates an interrupt to the processor associated with the process

4. (original) The notification mechanism set forth in claim 1, wherein a verb modifies an association of the at least one completion queue associated with at least one of the plurality of completion queue handlers.

5. (original) The notification mechanism set forth in claim 1, wherein a verb creates the at least one completion queue associated with at least one of the plurality of completion queue handlers.

6. (original) The notification mechanism set forth in claim 1, wherein a verb returns a number of the plurality of completion queue handlers that are associated with the communication device.

7. (original) The notification mechanism set forth in claim 1, wherein each of the plurality of completion queue handlers are associated with at least one completion queue through a completion queue handler identifier.

8. (Currently amended) A network, comprising:

a plurality of systems;

a switch network that connects the plurality of systems for communication; and

at least one of the plurality of systems, wherein the at least one of the plurality of systems comprises:

a communication device having a plurality of completion queues; and

at least two completion handlers associated with the communication device, wherein each completion handler is associated with one of a plurality of processes and associated with at least one of the plurality of completion queues, wherein the at least two completion queue handlers are segregated to target processors, and wherein the segregation of the at least two completion queue handlers is adapted to reduce cache line invalidation, cache line eviction, and/or unnecessary memory bus overhead associated with synchronization of accesses to the memory.

9. (original) The network set forth in claim 8, wherein the plurality of completion queues are associated with a plurality of queues.

10. (original) The network set forth in claim 8, wherein a first of at least two completion handlers is associated with one of the plurality of processes and a second of the at least two completion handlers is associated with another of plurality of processes.

11. (original) The network set forth in claim 10, wherein the first of at least two completion handlers communicates a first interrupt to a first processor associated with one of the plurality of processes and the second of the at least two completion handlers communicates a second interrupt to a second processor associated with another of the plurality of processes.

12. (original) The network set forth in claim 10, wherein a verb modifies the association of the first of at least two completion handlers with one of the plurality of processes.

13. (original) The network set forth in claim 8, wherein the at least two completion handlers reside in memory in the communication device.

14. (original) The network set forth in claim 8, wherein the at least two completion handlers reside in memory at least one of the plurality of systems that is external to the communication device.

15. (Currently amended) A method for providing notification to a plurality of processes, the method comprising the acts of:

creating a plurality of completion queues on a communication device, each of the plurality of completion queues associated with at least one of a plurality of completion queue handlers that are associated with the communication device, wherein each of the plurality of completion queue handlers are associated with one of a plurality of processes, wherein the plurality of completion queue handlers are segregated to target processors, and wherein the segregation of the plurality of the completion queue handlers is adapted to reduce cache line invalidation, cache line eviction, and/or unnecessary memory bus overhead associated with synchronization of accesses to the memory;

placing a completion queue entry on one of the plurality of completion queues;

invoking one of the plurality of completion queue handlers associated with the one of the plurality of completion queues; and

notifying the one of a plurality of processes associated with the one of a plurality of completion queue handlers.

16. (Previously amended) The method set forth in claim 15, comprising executing a plurality of processes on a plurality of processors.

17. (original) The method set forth in claim 15, comprising issuing a verb to return a number of the plurality of completion queue handlers that are associated with the communication device.

18. (Previously amended) The method set forth in claim 15, wherein the notification comprises the one of a plurality of completion queue handlers sending an interrupt to one of a plurality of processors.

19. (original) The method set forth in claim 15, comprising issuing a verb to create one of the plurality of completion queues.

20. (original) The method set forth in claim 15, comprising modifying the at least one of the plurality of completion queues through the issuance of a verb to modify the association of at least one of the plurality of completion queues with at least one of a plurality of completion queues.

21. (original) The method set forth in claim 15, wherein the creation of the plurality of completion queues comprises defining each of the plurality of completion queues in a memory.